

1 The Examiner's rejection of dependent claim 11 also relies upon U.S. Patent No. 5,937,320
2 ("Andricacos").

3 In rejecting apparatus claims 1-12, the Examiner has argued that it would have been
4 obvious to form the claimed apparatus by modifying Farnworth's integrated circuit structure by
5 creating triple metal layers to form bump electrodes in the manner taught by Hosomi. In
6 support of such rejection, the Examiner states that Farnworth's integrated circuit structure
7 includes a "semiconductor wafer (fig 1 and fig 2 numeral 16) having an upper surface, the
8 semiconductor wafer having a plurality of identical die (fig 1 numeral 18) formed inside."
9 However, Applicants submit that the Examiner has misunderstood the Farnworth disclosure. In
10 Figs. 1 and 2 of Farnworth, the semiconductor wafer is identified by reference numeral 12, and
11 not by reference numeral 16. Item 16 is instead an interconnect substrate which does not
12 include identical die; see Farnworth, col. 3, lines 25-37. Interconnect substrate 16 is used to
13 make temporary, rather than permanent, contact with electrode pads on separate semiconductor
14 wafers. Also, the Examiner states in the Office Action that Farnworth's structure includes "a
15 patterned layer of interconnect metal (fig 2 layer 32) formed upon the upper surface of the
16 semiconductor wafer ...". However, Farnworth's metal layer identified by reference numeral 32
17 represents "conductors 32 formed on the interconnect substrate 16" (see Farnworth, col. 4, lines
18 20-22), and not any interconnect metal formed upon semiconductor wafer 12. Likewise, the
19 connection pads 26 referenced by the Examiner within the Office Action are contact pads
20 formed on interconnect substrate 16, and not pads formed on semiconductor wafer 12. In
21 contrast, the "patterned layer of interconnect metal" recited by pending claim 1 is "formed upon
22 the upper surface of the semiconductor wafer". Thus, Farnworth does not disclose or suggest a
23 patterned layer of interconnect metal upon the upper surface of the semiconductor wafer itself.

24 The Examiner concedes within the Office Action that Farnworth does not mention the
25 formation of a triple metal layer to form bump electrodes. The Examiner therefore relies upon
26 Hosomi and argues that it would have been obvious to substitute the barrier metal layer (5) of
27 Hosomi, formed of thin metal films 5a, 5b, and 5c, in place of Farnworth's interconnect metal
28 layer 32. Even if such a combination of the references were "obvious", as contended by the

1 Examiner, the resulting substitution would not provide Applicants' claimed invention. Claim 1
2 calls for a patterned layer of interconnect metal formed upon the upper surface of the
3 semiconductor wafer including connection pads; a patterned layer of nickel plated over each
4 connection pad; a patterned layer of palladium plated over the patterned layer of nickel above
5 each connection pad; and a patterned layer of gold plated over the patterned layer of palladium
6 above each connection pad. Thus, even if the interconnect metal layer 32 formed by Farnworth
7 on interconnect substrate 16 were replaced by Hosomi's barrier metal layer 5, the resulting
8 stacked metal structure would not be formed upon the upper surface of the semiconductor
9 wafer, as recited by pending claim 1.

10 Even if it were argued that it was somehow obvious to form Hosomi's barrier metal
11 layer 5 upon interconnect pads disposed upon the upper surface of an actual semiconductor
12 wafer containing a plurality of identical die, claim 1, as amended above, requires that the
13 patterned layer of nickel be "in direct contact with the underlying connection pads" that are
14 formed by the patterned layer of interconnect metal that is provided upon the upper surface of
15 the semiconductor wafer. In contrast, Hosomi teaches that a titanium (Ti) layer 5a is formed
16 over electrode pad 2, and then a nickel (Ni) layer 5b is formed over the titanium layer 5a.
17 Hosomi's titanium layer 5a therefore prevents nickel layer 5b from being in direct contact with
18 the underlying aluminum electrode pad 2. Thus, the use of Hosomi's barrier metal layer 5 over
19 an interconnect metal layer of a semiconductor wafer nonetheless fails to provide the invention
20 recited by claim 1.

21 Pending dependent claims 2-5 and 7-12 all depend from claim 1; accordingly, all of
22 such dependent claims should be allowable for the same reasons set forth above in regard to
23 claim 1.

24 Pending process claims 13-17 and 19-24 have been rejected by the Examiner under 35
25 U.S.C. §103(a) as describing subject matter considered by the Examiner to be obvious from
26 Farnworth in view of Hosomi and Andricacos. The Examiner cited Andricacos to support the
27 argument that it would have been obvious to use electroless plating to form the barrier metal
28 layers of Hosomi. However, claim 13 recites a process including the step of forming a

1 patterned layer of gold by electroless plating over the patterned layer of palladium above each
2 connection pad. The Hosomi process includes the formation of a gold (Au) bump, identified by
3 reference numeral 6 in Fig. 1; gold bump 6 of Hosomi is used for mounting a semiconductor
4 device to a TAB (tape-automated-bonding) tape. It is simply not possible to use the method of
5 electroless plating for gold deposition, and still achieve the thickness that is required to form
6 gold bump 6. It would therefore not be obvious to modify the fabrication process described by
7 Hosomi to use electroless plating to form Hosomi's gold bump 6.

8 In conjunction with the Examiner's rejection of claim 13, the Examiner again argues (at
9 page 6 of the Office Action) that Farnworth's integrated circuit structure includes a
10 "semiconductor wafer (fig 1 and fig 2 numeral 16) ... having a plurality of identical die (fig 1
11 numeral 18) formed inside", as well as "a patterned layer of interconnect metal (fig 2 layer 32)
12 formed upon the upper surface of the semiconductor wafer ...". Applicants have already noted
13 above that reference numeral 16 is an interconnect substrate rather than a semiconductor wafer
14 having a plurality of identical die, and that Farnworth's metal layer 32 are conductors formed
15 on interconnect substrate 16. In addition, Applicants have already pointed out that the
16 connection pads 26 again referenced by the Examiner on page 6 of the Office Action are contact
17 pads formed on interconnect substrate 16, and not pads formed on semiconductor wafer 12. In
18 contrast, claim 13 recites the step of forming a patterned layer of interconnect metal upon the
19 upper surface of the semiconductor wafer that contains the plurality of identical die. Thus,
20 Farnworth does not disclose or suggest a process that includes the step of forming a patterned
21 layer of interconnect metal upon the upper surface of the semiconductor wafer itself.

22 Once again, even if it would somehow have been obvious to form Hosomi's barrier
23 metal layers 5a, 5b, and 5c above Farnworth's interconnect metal layer 32, the result would not
24 provide or suggest the process recited by pending claim 13. Claim 13 recites a process
25 including the step of forming a patterned layer of interconnect metal upon the upper surface of
26 the semiconductor wafer, thereby providing connection pads, and then forming a patterned layer
27 of nickel by electroless plating over each connection pad. Thus, even if Hosomi's process of
28 forming barrier metal layer 5 were applied over the interconnect metal layer 32 formed by

1 Farnworth on interconnect substrate 16, the resulting process would not be practiced upon the
2 upper surface of the semiconductor wafer, as recited by pending claim 13.

3 Similarly, even if it were argued that it was somehow obvious to apply Hosomi's barrier
4 metal layer process over interconnect pads disposed upon the upper surface of an actual
5 semiconductor wafer containing a plurality of identical die, claim 13, as amended above,
6 requires the step of electroless plating the nickel layer over each connection pad such that the
7 patterned layer of nickel is in direct contact with the underlying connection pads. However, as
8 mentioned above, Hosomi requires that a titanium (Ti) layer 5a be formed over aluminum
9 electrode pad 2 before the nickel (Ni) layer 5b is formed over the titanium layer 5a. Thus,
10 Hosomi's titanium layer 5a prevents nickel layer 5b from being in direct contact with Hosomi's
11 underlying aluminum electrode pad 2, as contrasted with the process recited by claim 13.

Pending dependent claims 14-17 and 19-24 all depend from claim 13; accordingly, all of such dependent claims should be allowable for the same reasons set forth above in regard to claim 13.

Having now fully responded to the Office Action, Applicants respectfully submit that the pending claims patentably distinguish over the cited references, and that the application is now in condition for allowance, which action is earnestly requested.

18 || Respectfully submitted,

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ATTACHMENT A

1 We claim:

- 2 1. An integrated circuit structure comprising in combination:
 - 3 a. a semiconductor wafer having an upper surface, the semiconductor wafer having a
4 plurality of identical die formed therein, each of the identical die having a plurality of semiconductor
5 devices formed therein upon the surface of the semiconductor wafer;
 - 6 b. a patterned layer of interconnect metal formed upon the upper surface of the
7 semiconductor wafer for electrically interconnecting the plurality of semiconductor devices formed
8 within each such die, said patterned layer of interconnect metal including connection pads for
9 making electrical connection to circuitry external to the semiconductor wafer;
 - 10 c. a patterned layer of nickel plated over each connection pad for mechanically and
11 electrically bonding to the interconnect metal forming such connection pad, the patterned layer of
12 nickel being in direct contact with the underlying connection pads;
 - 13 d. a patterned layer of palladium plated over the patterned layer of nickel above each
14 connection pad for preventing the nickel from diffusing outwardly through the palladium during
15 subsequent heating cycles; and
 - 16 e. a patterned layer of gold plated over the patterned layer of palladium above each
17 connection pad to facilitate the joinder of such connection pad with a connection element.

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19 2. The integrated circuit structure recited by claim 1 wherein said connection element is a
20 gold bump.

21

22 3. The integrated circuit structure recited by claim 1 wherein said connection element is a
23 gold wire bond.

24

25 4. The integrated circuit structure recited by claim 1 wherein said connection element is a
26 solder bump.

27

28 5. The integrated circuit structure recited by claim 1 wherein said connection element is a

1 nickel bump.

2
3 7. The integrated circuit structure recited by claim 1 wherein, upon each of said die, two of
4 said connection pads are disposed within 5 micrometers of each other.

5
6 8. The integrated circuit structure recited by claim 1 wherein said patterned layer of nickel
7 has a thickness that lies in the range of 0.5 micrometers and 20 micrometers.

8
9 9. The integrated circuit structure recited by claim 1 wherein said patterned layer of
10 palladium has a thickness that lies in the range of 0.1 micrometers and 5 micrometers.

11
12 10. The integrated circuit structure recited by claim 1 wherein said patterned layer of gold has
13 a thickness that lies in the range of 0.03 micrometers and 2 micrometers.

14
15 11. The integrated circuit structure recited by claim 1 wherein said patterned layer of
16 interconnect metal is formed of copper.

17
18 12. The integrated circuit structure recited by claim 1 wherein said patterned layer of
19 interconnect metal is formed of aluminum.

20
21 12. A process for forming connection pads on a plurality of integrated circuit die formed in a
22 semiconductor wafer, the semiconductor wafer having an upper surface, each of the integrated circuit
23 die having a plurality of semiconductor devices formed therein upon the surface of the
24 semiconductor wafer, said process including the steps of:

25 a. forming a patterned layer of interconnect metal upon the upper surface of the
26 semiconductor wafer for electrically interconnecting the plurality of semiconductor devices formed
27 within each such integrated circuit die, said patterned layer of interconnect metal including
28 connection pads for making electrical connection to circuitry external to the semiconductor wafer;

- 1 b. following step a., forming a patterned layer of nickel by electroless plating over each
2 connection pad for mechanically and electrically bonding to the interconnect metal at each such
3 connection pad, the patterned layer of nickel being in direct contact with the underlying connection
4 pads;
- 5 c. following step b., forming a patterned layer of palladium by electroless plating over the
6 patterned layer of nickel above each connection pad for preventing the nickel from diffusing
7 outwardly through the palladium during subsequent heating cycles; and
- 8 d. following step c., forming a patterned layer of gold by electroless plating over the
9 patterned layer of palladium above each connection pad to facilitate the joinder of such connection
10 pad with a connection element.

11

12 13 14. The process recited by claim 19 including the further step of joining a gold bump to the
13 patterned layer of gold above at least one of said connection pads.

14

15 14. The process recited by claim 19 including the further step of joining a gold wire bond to
16 the patterned layer of gold above at least one of said connection pads.

17

18 15. The process recited by claim 19 including the further step of joining a solder bump to the
19 patterned layer of gold above at least one of said connection pads.

20

21 16. The process recited by claim 19 including the further step of joining a nickel bump to the
22 patterned layer of gold above at least one of said connection pads.

23

24 18. The process recited by claim 19 wherein, upon each of said integrated circuit die, at least
25 two of the connection pads are formed within 5 micrometers of each other.

1 19. ~~20~~¹². The process recited by claim ~~13~~ wherein said step of forming a patterned layer of nickel
2 produces a nickel layer having a thickness that lies in the range of 0.5 micrometers and 20
3 micrometers.

4
5 20. ~~21~~¹². The process recited by claim ~~13~~ wherein said step of forming a patterned layer of
6 palladium produces a palladium layer having a thickness that lies in the range of 0.1 micrometers and
7 5 micrometers.

8
9 21. ~~22~~¹². The process recited by claim ~~13~~ wherein said step of forming a patterned layer of gold
10 produces a gold layer having a thickness that lies in the range of 0.03 micrometers and 2
11 micrometers.

12
13 22. ~~23~~¹². The process recited by claim ~~13~~ wherein said step of forming a patterned layer of
14 interconnect metal upon the upper surface of the semiconductor wafer for electrically interconnecting
15 the plurality of semiconductor devices includes the step of forming such patterned layer of
16 interconnect metal from the metal copper.

17
18 23. ~~24~~¹². The process recited by claim ~~13~~ wherein said process includes the further step of heating
19 the semiconductor wafer following the step of forming the patterned layer of gold in order to thermal
20 cycle the plurality of semiconductor devices formed within each such integrated circuit die.

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